APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,983	07/30/2001	Paul Mantey	10016250-1	9739

			EXAMINER
22879	7590	09/27/2004	COLEMAN, ERIC

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/917,983	MANTEY ET AL.
	Examiner	Art Unit
	Eric Coleman	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *14-18* is/are allowed.

6)☒ Claim(s) *1-6,8-10,13* is/are rejected.

7)☐ Claim(s) *7,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____ .

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

DETAILED ACTION

Specification

1.   The applicant is advised that the Related Applications section of the specification

(on page 1) should be updated as appropriate.

Claim Rejections - 35 USC § 112

2.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of
> making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the
> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall
> set forth the best mode contemplated by the inventor of carrying out his invention.

3.   Claims 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. Claims 8 and 9 are written as one paragraph and

therefore it is unclear if the limitations of 8 and 9 are separate or not. Therefore the

scope of meaning of claims 8 and 9 is unclear.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by
> another filed in the United States before the invention by the applicant for patent or (2) a patent
> granted on an application for patent by another filed in the United States before the invention by the
> applicant for patent, except that an international application filed under the treaty defined in section
> 351(a) shall have the effects for purposes of this subsection of an application filed in the United States
> only if the international application designated the United States and was published under Article 21(2)
> of such treaty in the English language.

5.   Claims 1-4,6,8-10,13 are rejected under 35 U.S.C. 102(e) as being anticipated

by Lin (patent No. 6,651,225).

6.   Lin taught the invention as claimed including a data processing ("DP") system

comprising:

        a) Plurality of programmable logic devices including at least a first and second

programmable logic device (field programmable processor array chips) (e.g., see figs.

8,10,22,24,39,40a, 40b, 42, 44, 56, 69, 74, 86, 87, 88) the programmable logic devices

coupled to receive programmable logic device configuration code from a first and

second memory (1205,1206,SRAM H, SRAM L) (e.g., see fig. 3,6,22,42,56.69 and col.

13 lines27-49, and col. 115, lines 44-65 and col. 119, lines 1-55)(as to the type of

memory in the embodiment being SRAM, Lin taught that the memory type may be

DRAM flash or EEPROM, e.g., see col. 120, line 63-col. 121, line 12);

        b) First serial bus (FD bus on board 1 of fig. 69) coupling the memory (SRAM or

EEPROM e.g., see col. 120, line 63-col. 121, line 12) with common configuration logic

(700,2145)(e.g., see col. 149, lines 15-21 and figs.22, 69), and second serial bus

coupling the second memory (SRAM or EEPROM) (with the common configuration logic

(e.g., see figs.10,22, 56,69);

        c) Processor coupled to the common configuration logic, wherein the processor

is also coupled a memory subsystem (e.g., see figs. 1, 69);

        d) Wherein the processor is capable or transferring programmable logic

configuration code to its memory subsystem into the first memory (SRAM or

EEPROM)(e.g., see col. 117, lines 47-65).

7.   As per claim 2, Lin taught the plurality of separate boards each with plural

FPGAs and memories (SRAM or EEPROM) (e.g., see fig. 69).

8.   As per claim 3, Lin taught use of the JTAG interfaces with the buses (e.g., see

col. 70, lines 5-35) which would require the buses connected to the JTAG interfaces to

perform as JTAG buses.

9.   As per claim 4, Lin taught a third bus (2171) for connecting the processor to the

common configuration logic (e.g., see fig.22, 69).

10.   As per claims 6,8,9,13 Lin taught the programmable logic devices comprised field

programmable gate array (e.g., see figs. 8,10,22,56,69, and col. 4, lines 1-27) and the

common configuration logic comprised a field programmable gate array that is coupled

to memory containing configuration code (e.g., see col. 149, lines 48-65).

11.   As per claim 10, Lin taught transferring the configuration code from a server via a

network interconnect to the common control logic and into the memory (SRAM or

EEPROM). (e.g., see figs. 1,66,69 and col. 11 line 47-col. 13, line 62).

Claim Rejections - 35 USC § 103

12.   Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin

(patent No. 6,651,225).

Lin taught the invention substantially as claimed including a data processing

("DP") system comprising:

a) Plurality of programmable logic devices including at least a first and second

programmable logic device (field programmable processor array chips) (e.g., see figs.

8,10,22,24,39,40a, 40b, 42, 44, 56, 69, 74, 86, 87, 88) the programmable logic devices

coupled to receive programmable logic device configuration code from a first and

second memory (1205,1206,SRAM H, SRAM L) (e.g., see fig. 3,6,22,42,56.69 and col.

13 lines27-49, and col. 115, lines 44-65 and col. 119, lines 1-55)(as to the type of

memory in the embodiment being SRAM, Lin taught that the memory type may be

DRAM flash or EEPROM, e.g., see col. 120, line 63-col. 121, line 12);

b) First serial bus (FD bus on board 1 of fig. 69) coupling the memory (SRAM or

EEPROM e.g., see col. 120, line 63-col. 121, line 12) with common configuration logic

(700,2145)(e.g., see col. 149, lines 15-21 and figs.22, 69), and second serial bus

coupling the second memory (SRAM or EEPROM) (with the common configuration logic

(e.g., see figs.10, 22, 56,69);

c) Processor coupled to the common configuration logic, wherein the processor

is also coupled a memory subsystem (e.g., see figs. 1, 69);

d) Wherein the processor is capable or transferring programmable logic

configuration code to its memory subsystem into the first memory (SRAM or

EEPROM)(e.g., see col. 117, lines 47-65).

13.   As per claim 2, Lin taught the Plurality of separate boards each with plural

FPGAs and memories (SRAM or EEPROM) (e.g., see fig. 69).

14.   As per claim 3, Lin taught use of the JTAG interfaces with the buses (e.g., see

col. 70, lines 5-35) which would require the buses connected to the JTAG interfaces to

perform as JTAG buses.

15.   As per claim 4, Lin taught a third bus (2171) for connecting the processor the

common configuration logic (e.g., see fig.22, 69);

16.   As per claim 5, the use of IIC type buses for connecting system elements to

EEPROMs was well known in the art at the time of the claimed invention and are readily

available as expressly admitted by applicant on pages 1 and 2 of the specification in the

instant application. The specification indicates (in pages 1 and 2) that these buses

separate the clock and data; and operate with a single bus master and eliminate the

need for complicated timing elements. Lin taught a system where the processor was

connected to the common configuration control through a bus where there was no other

elements connected to the bus (2171) (e.g., see fig. 69) therefore one of ordinary skill

would have been motivated to use a IIC type bus at least to eliminate the need for

complicated timing elements to control the bus.

Allowable Subject Matter

17.   Claim 7,11,12 is objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations of the

base claim and any intervening claims.

18.   Claims 14-18 are allowed.

Conclusion

19.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

Liu (patent No. 5,425,036) disclosed a system for debugging reconfigurable

emulation systems.

Hsieh (patent No. 5,428,800) disclosed a input/output (I/O) bi-directional buffer

for interfacing (I/O ports of a field programmable interconnection device (e.g., see

abstract).

Hsieh (patent No. 5,465,056) disclosed system for programmable and signal switching (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674 or (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER